IN THE CLAIMS

1 (Previously Amended). A semiconductor stacking structure comprising:

a semiconductor die;

a flexible tape substrate having at least one metal layer~~s~~ for electrical connections wherein the flexible tape substrate is coupled to a bottom surface of the semiconductor die;

wirebonds for electrically coupling the semiconductor die to the metal layer; and

an encapsulant covering the semiconductor die and the wirebonds;

wherein the flexible tape substrate further comprises a plurality of flap portions and each flap portion is folded along a side surface and an upper surface of the encapsulant;

wherein the flap portions do not over lap one another and cover only a portion of the upper surface of the encapsulant;

wherein the folded flap portions have an exposed metal layer.

2 (Previously Presented). A semiconductor stacking structure in accordance with Claim 1 further comprising an adhesive layer which is placed on the flap portions of the flexible tape substrate and which couples the flap portions to the upper surface of the encapsulant.

3 (Previously Presented). A semiconductor stacking structure in accordance with Claim 1 further comprising an adhesive layer which is placed on the upper surface of the encapsulant and which couples the flap portions to the encapsulant.

4 (Previously Presented). A semiconductor stacking structure in accordance with Claim 1 further comprising a semiconductor device coupled to the flap portions of the flexible tape substrate.

5 (Previously Presented). A semiconductor stacking structure in accordance with Claim 4 wherein the semiconductor device is coupled to the flap portions of the flexible tape substrate after the flap portions are folded over and coupled to the encapsulant.

6 (Previously Presented). A semiconductor stacking structure in accordance with Claim 4 wherein the semiconductor device is coupled to the flap portions of the flexible tape substrate before the flap portions are folded over and coupled to the encapsulant.

7 (Original). A semiconductor stacking structure ~~package~~ in accordance with Claim 1 wherein the semiconductor stacking structure is a LGA (Land Grid Array) device.

8 (Original). A semiconductor stacking structure in accordance with Claim 1 wherein the semiconductor stacking structure is a BGA (Ball Grid Array) device.

9 (Original). A semiconductor stacking structure in accordance with Claim 1 wherein the semiconductor stacking structure is a lead type of device.

10 (Previously Presented). A semiconductor stacking structure in accordance with Claim 1 wherein the flexible tape substrate is folded over on four sides to form flap portions which are coupled to the upper surface of the encapsulant and covers only a portion of the upper surface of the encapsulant.

11 (Previously Presented). A semiconductor stacking structure comprising:

a semiconductor die;

means for interconnection having at least one metal layers for electrical connections coupled to a bottom surface of the semiconductor die;

wirebonds for electrically coupling the semiconductor die to the metal layer; and

an encapsulant covering the semiconductor die and the wirebonds;

wherein the interconnection means further comprises a plurality of flap portions and each flap portion is folded along a side surface and an upper surface of the encapsulant;

wherein the flap portions do not over lap one another and cover only a portion of the upper surface of the encapsulant;

wherein the folded flap portions have an exposed metal layer.

12 (Previously Presented). A semiconductor stacking structure in accordance with Claim 11 further comprising an adhesive layer placed on the means for coupling the interconnection means to the upper surface of the encapsulant.

13 (Previously Cancelled).

14 (Previously Cancelled).

15 (Previously Cancelled).

16 (Previously Cancelled).

17 (Previously Cancelled).

18 (Previously Cancelled).

19 (Previously Cancelled).

20 (Previously Cancelled).

21 (Previously Presented). A semiconductor stacking structure comprising:

a semiconductor die;

means for interconnection having at least one metal layers for electrical connections coupled to a bottom surface of the semiconductor die;

wirebonds for electrically coupling the semiconductor die to the metal layer; and

an encapsulant covering the semiconductor die and the wirebonds;

wherein the interconnection means further comprises at least four flap portions and each flap portion is folded along a side surface and an upper surface of the encapsulant;

wherein the flap portions do not over lap one another and cover only a portion of the upper surface of the encapsulant;

wherein the folded flap portions have an exposed metal layer.

22 (Previously Presented). A semiconductor stacking structure in accordance with Claim 21 further comprising means placed on the flap portions of the flexible substrate for coupling the flap portions to the encapsulant.

23 (Previously Presented). A semiconductor stacking structure in accordance with Claim 21 further comprising means placed on the upper surface of the encapsulant for coupling the flap portions to the encapsulant.

24 (Previously Presented). A semiconductor stacking structure in accordance with Claim 21 further comprising a semiconductor device coupled to the flap portions of the coupling means.

25 (Previously Presented). A semiconductor stacking structure in accordance with Claim 24 wherein the semiconductor device is coupled to the flap portions of the coupling means after the flap portions are folded over and coupled to the encapsulant.

26 (Previously Presented). A semiconductor stacking structure in accordance with Claim 24 wherein the semiconductor device is coupled to the flap portions of the coupling means before the flap portions are folded over and coupled to the encapsulant.

27 (Previously Cancelled).

28 (Previously Cancelled).

29 (Previously Added). A semiconductor stacking structure in accordance with Claim 1 further comprising an adhesive for coupling the semiconductor die to the flexible tape substrate.

30 (Previously Added). A semiconductor stacking structure in accordance with Claim 11 further comprising an adhesive for coupling the semiconductor die to the means.